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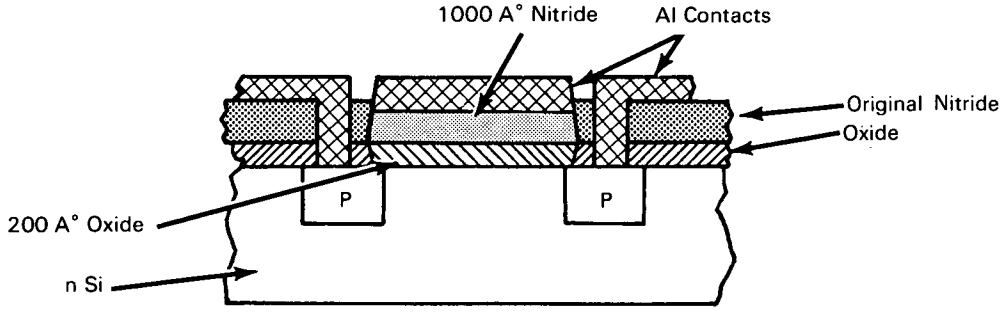
NASA TECH BRIEF

Radiation Tolerant Silicon Nitride Insulated Gate Field Effect Transistors



Metal-Nitride-Semiconductor Field Effect Transistor Structure

MISFET (Metal-Insulated-Semiconductor Field Effect Transistor) devices have been fabricated using a silicon nitride passivation layer on top of a thermally grown thin silicon oxide layer. The addition of the nitride layer has been shown to enhance the radiation tolerance of the MISFET device. This multi-layer dielectric structured device is very attractive in electronic systems which will be exposed to the space radiation environment or the effects of nuclear weapons. The technology should be of interest to manufacturers of semiconductors and solid state radiation monitoring equipment.

The problem:

When MIS devices fabricated with the conventional silicon oxide dielectric layer are exposed to an ionizing radiation environment such as that encountered in the Van Allen belts, they have been shown to exhibit a progressive deterioration of the electrical properties. This radiation sensitivity is manifested by a possible shift in the C-V and the I-V characteristics in the direction of higher negative voltages. Therefore, to reach a pre-irradiation drain current level it is necessary to bias the gate more negatively. Under electron irradiation the gate threshold voltage of commercial p-channel devices increases in value from below -5V to beyond -30V, depending on operating bias and radiation fluence. This increase requirement will generally make the device inoperative and result in circuit failure.

The solution:

The two most important physical changes occurring when MIS structures are exposed to ionizing radiation are (1) the introduction of a fixed positive oxide space charge by the occupation of pre-existing charge-trapping sites in the oxide and (2) the creation of new interface states at the silicon-silicon dioxide interface. The first effect can be greatly reduced by using silicon nitride as the dielectric which has an inherent low trap density and susceptibility to contamination during fabrication. The second effect can be alleviated by in-situ etching before thermal oxidation and prior heat treatment of the silicon wafer.

(continued overleaf)

How it's done:

The fabrication process variables to be considered are the silicon resistivity type and surface state conditions, the silicon nitride deposition conditions, the contact metallization procedure and the final encapsulation. The actual device, shown in Figure 1, is processed as follows:

The substrate for the device is a 10 ohm-cm, n-type slice of silicon 0.10 ± 0.001 inches thick and mechanically polished on one side. This slice is cleaned, etched and rinsed in deionized water and a silicon nitride layer about 1900 Å thick is then deposited at 900°C by the vapor phase pyrolysis of ammonia and silane.

The windows for the source and drain diffusions are cut into the silicon nitride layer by standard photoresist etching procedures and boron oxide is then deposited for the p - type source - drain junctions. The insulator material over the gate is removed completely and 200 Å of oxide is thermally grown in the reactor followed by 1000 Å of silicon nitride.

After this, the previously deposited boron is thermally diffused to a depth of 2.5 microns to form the source and drain junctions. Contact windows are then opened over the source and drain and aluminum is evaporated as the contact material. A heat treatment to partially alloy the Al in the source drain regions for lower contact resistance then follows to complete the fabrication process. The devices are individually mounted on four-lead TO-5 headers and subjected to electrical performance and radiation tolerance evaluations.

Note:

Documentation is available from:

Clearinghouse for Federal Scientific
and Technical Information
Springfield, Virginia 22151
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Patent status:

No patent action is contemplated by NASA.

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